A 15.5-mW 20-GSps 4-Bit Charge-Steering Flash ADC

MWSCAS'15

Authors:

Mostafa M. Ayesh

Sameh Ibrahim

Mohamed M. Aboudina

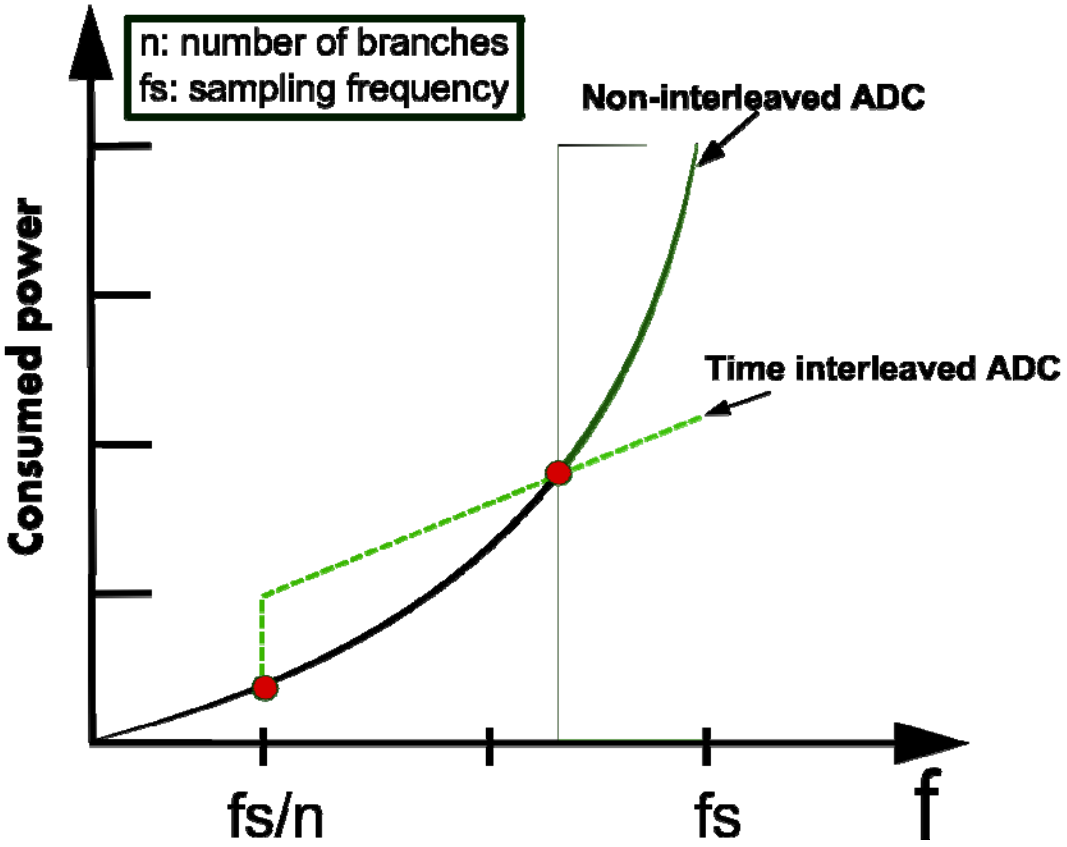
ALEXANDRIA UNIVERSITY

Outline

- Time-interleaving concept
- Low Power techniques
- ADC architecture
- Charge-steering concept
- Proposed comparator circuit
- Simulation results

- Time-interleaving Concept

- Overall power is reduced at higher data-rates

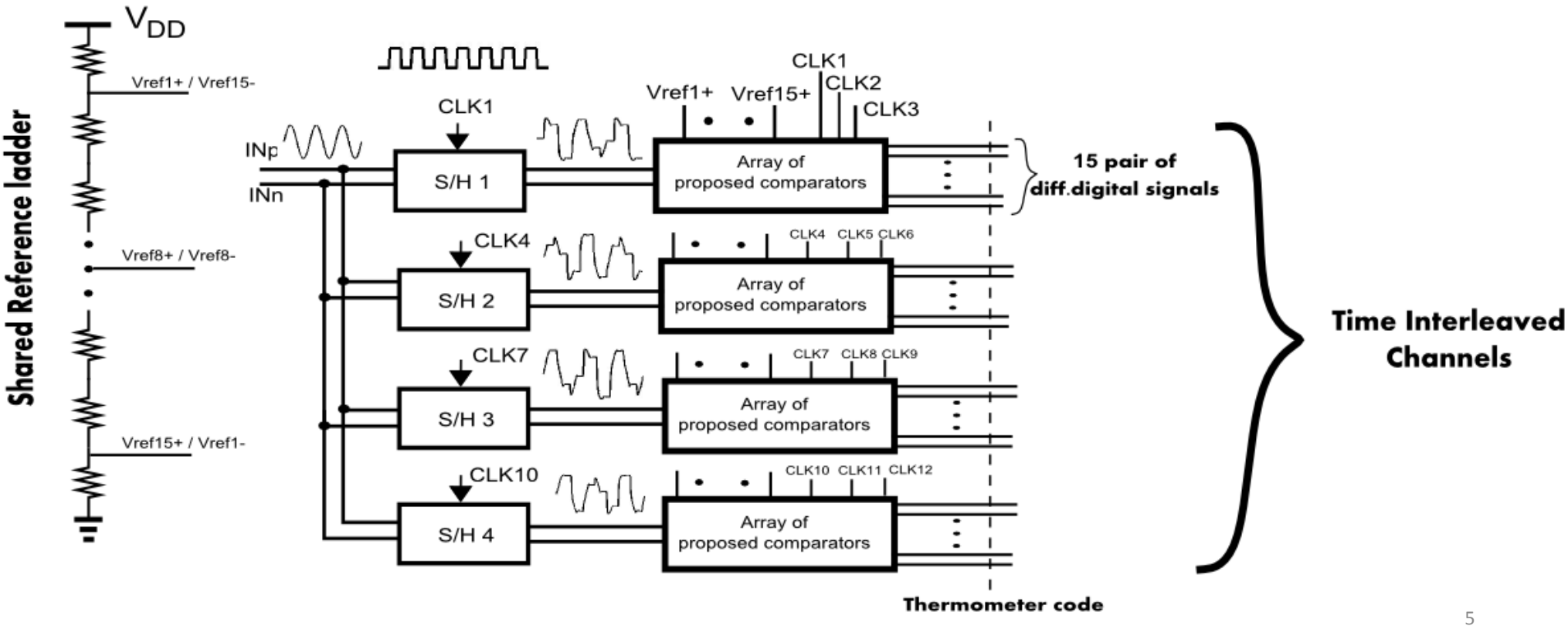


• Low-power Techniques

- Sharing the reference ladder between the four channels.
- Using charge-steering concept.
- Merging the regenerative latch inside the pre-amplifier.

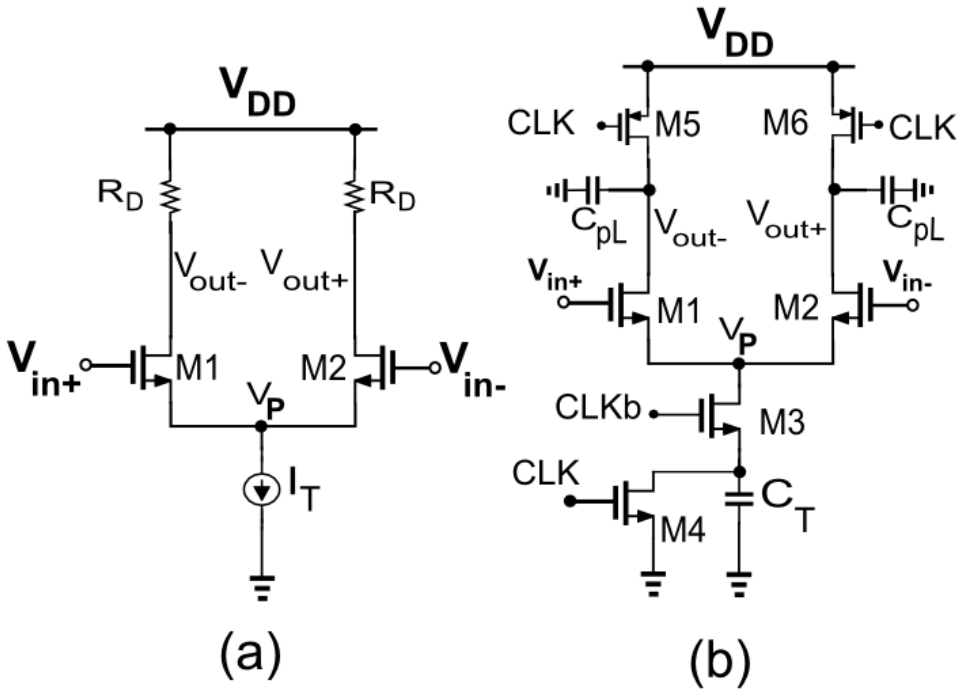
- High-speed Low-power Flash ADC

Overall ADC System



• Charge-steering Concept

- Charge-steering is using charge redistribution without the need of a DC path to GND.
- Ultra-low power technique



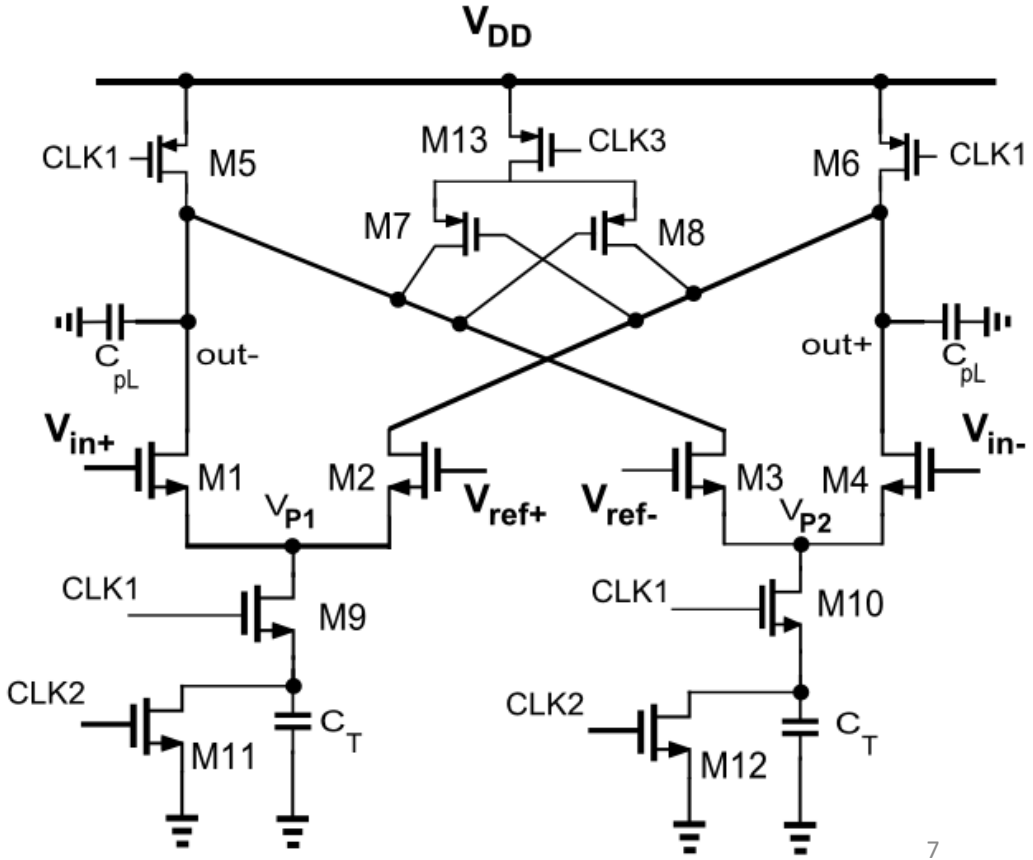
- High-speed Low-power Flash ADC
  Comparator – the basic unit –

- Circuit level:

  A novel design for the comparator is used.

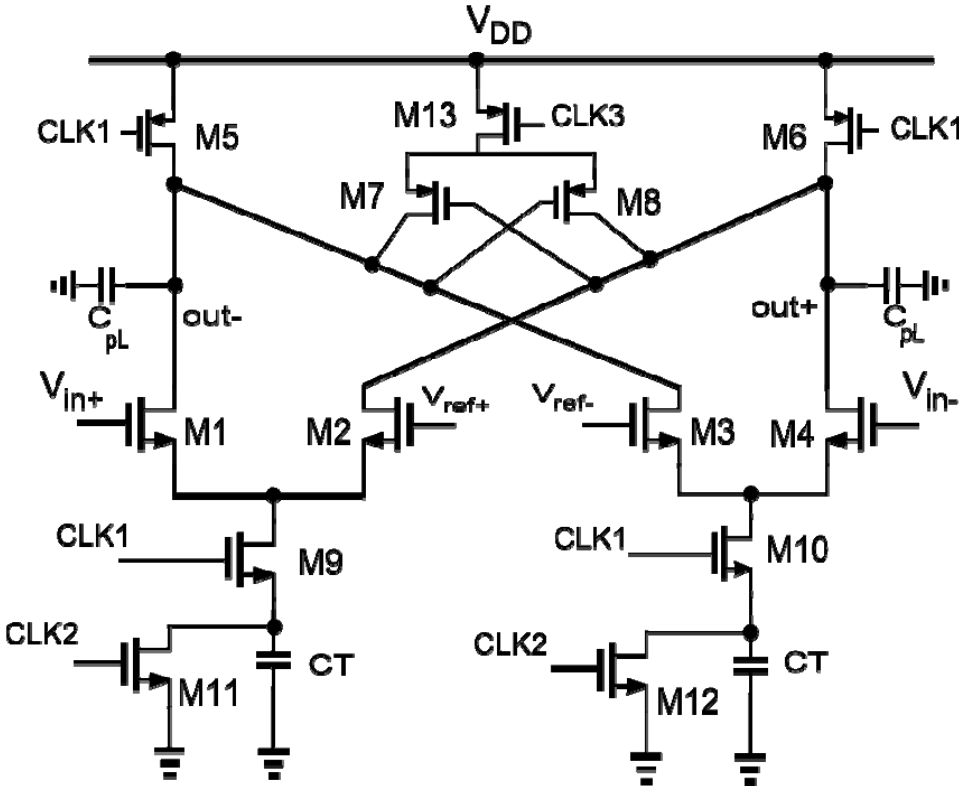
  Charge-steering based comparator

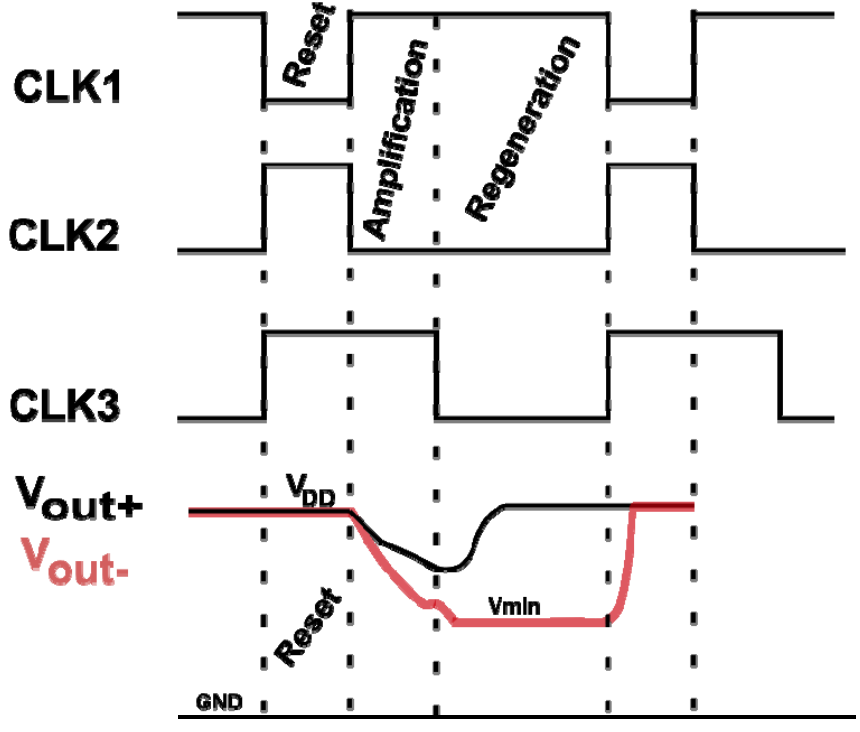
  Adv.
  - Ultra-low power
  - High speed
  - Low kick-back noise



- High-speed Low-power Flash ADC

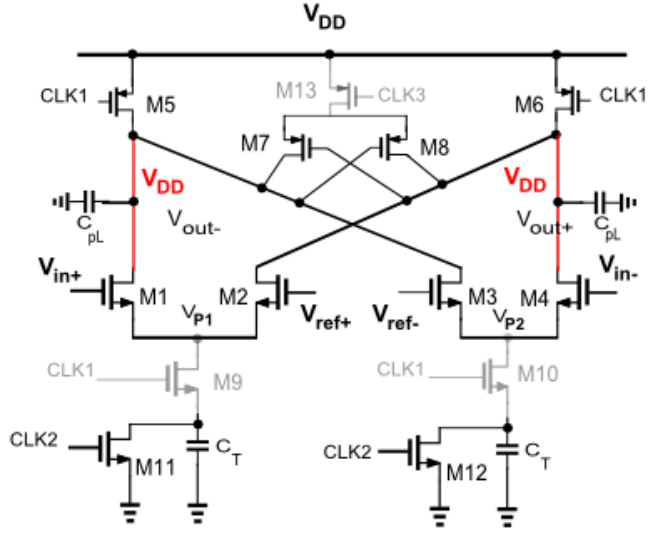
Comparator Circuit and Clocking Schemes



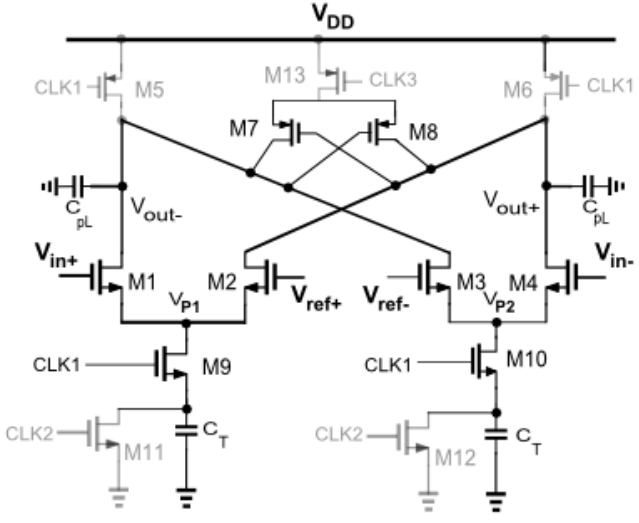


- High-speed Low-power Flash ADC

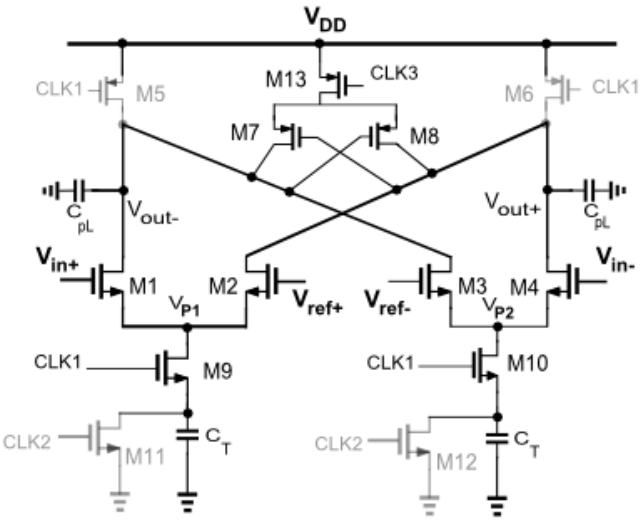
Comparator Different Phases of Operation



Reset phase



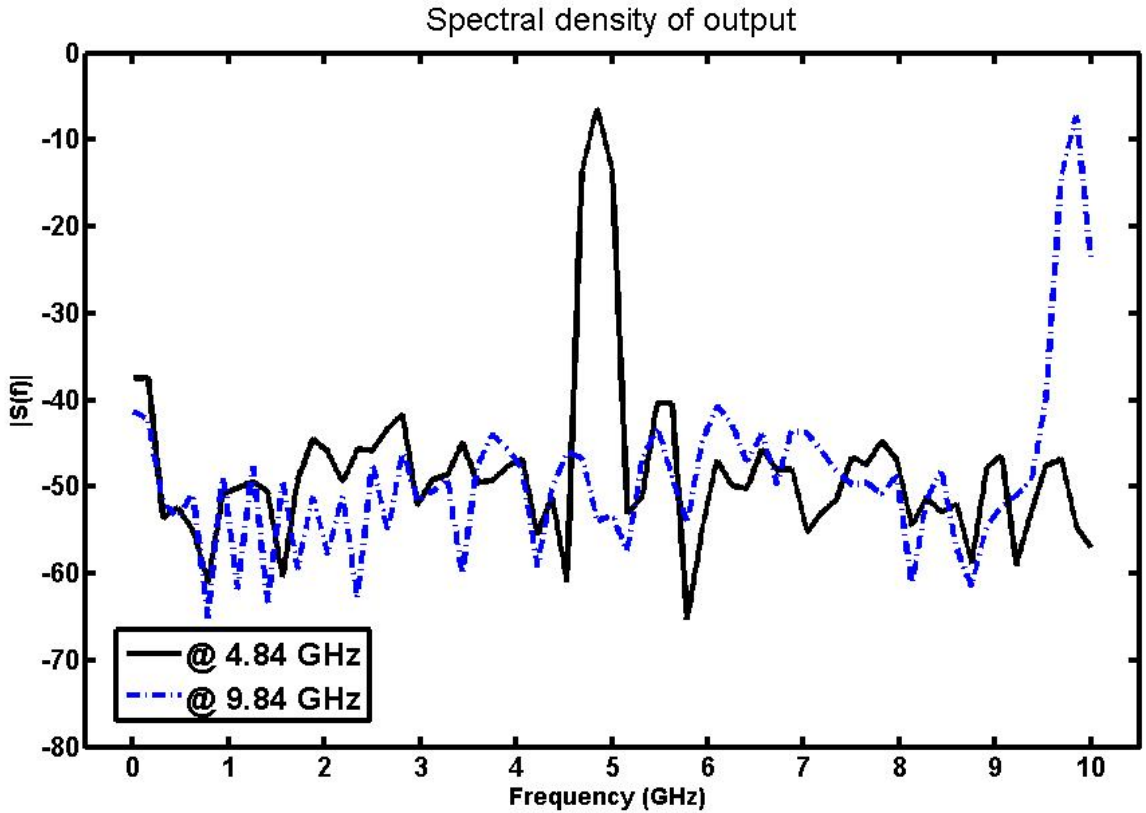
Amplification phase



Regeneration phase

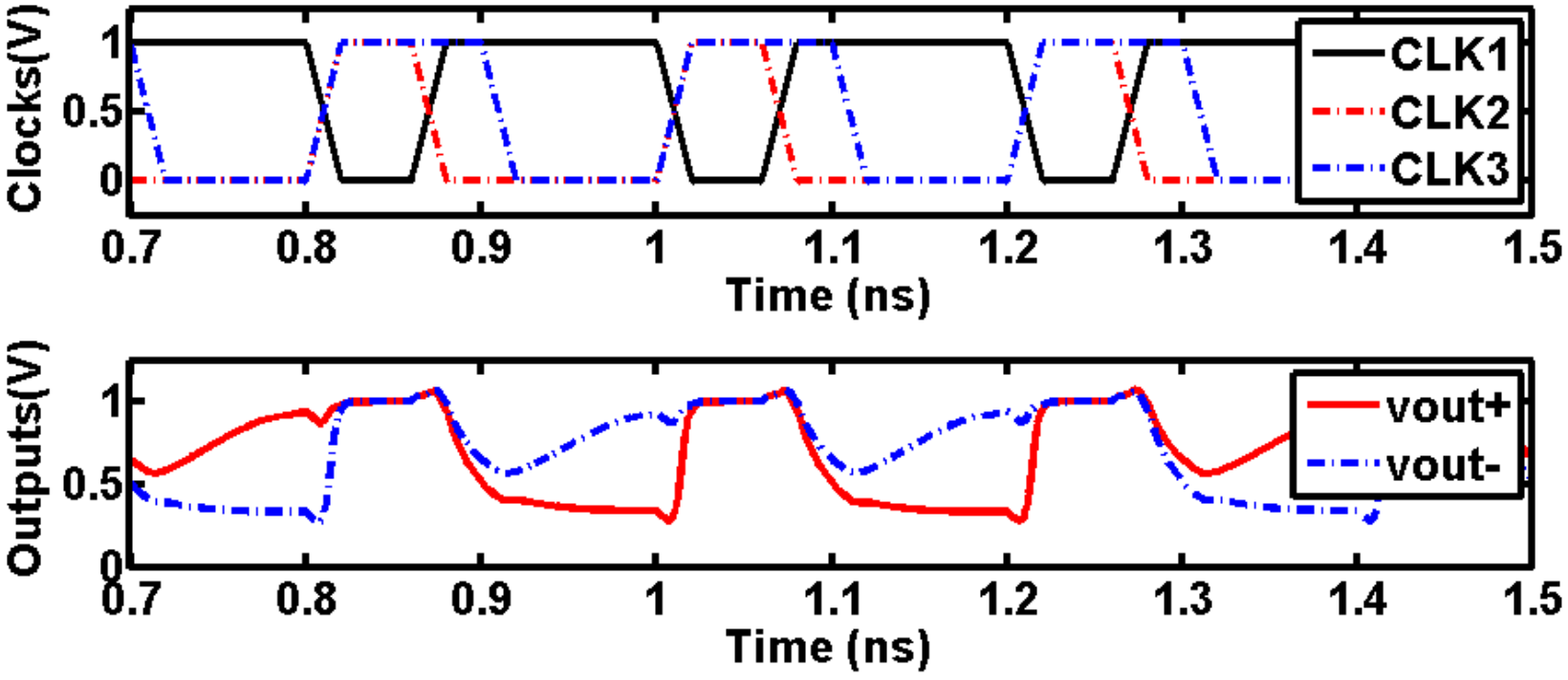
- High-speed Low-power Flash ADC

FFT for the Output of the ADC



- High-speed Low-power Flash ADC

  Transient Analysis for the Output of the ADC



- High-speed Low-power Flash ADC

Full ADC Simulation Results

Sampling frequency	**20 GSPS**
Input Range	**600 mVdiff**
SFDR	**33.58 dB**
SNDR	**23.86 dB**
ENOB (for 9.98GHz input frequency)	**3.67 Bits**
Power at Nyquist frequency	**15.5 mW**
FOMW*	**60.8 fJ/conv-step**

$$* \ FOMW = \frac{Power}{Sampling\ rate \ * 2^{ENOB}}$$