A Low-power High-speed Charge-steering ADC-based Equalizer for Serial Links

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Abstract

This thesis presents a 20-GSps low-power ADC based equalizer for high speed serial links receiver. The ADC-based equalizer is designed and simulated in a 65-nm CMOS technology and dissipates 15.5 mW in the ADC and 0.45 mW in the discrete time linear equalizer from 1-V supply. Low power consumption is achieved by using interleaving in ADC architecture, utilizing charge-steering concept, sharing single reference ladder across the four interleaved branches of ADC, and using a novel proposed design for the comparator itself in the Flash ADC besides using the novel DTLE circuit.

Introduction

The goal of the thesis is to design an ultra-low-power ADC-based equalizer with a 4-bit 20-GSps ADC. A 4x time-interleaved flash ADC is adopted to reduce consumed power as in **fig.1**. A new proposed ultra-low power comparator is used where charge steering concept is adopted. The proposed comparator merges the pre-amplifier and the regenerative latch into one block, while relying on charge re-distribution between different phases of operation to achieve pre-amplification and regeneration. Sharing the reference ladder between the interleaved branches while keeping the kickback noise at an acceptable level is also implemented and led to significant power reduction as well.

DTLE (Discrete-Time Linear Equalizer)

DTLE is a linear equalizer that replaces the conventional CTLE and its continuous nature to a discrete nature. It can be seen as a merged CTLE and S/H circuit. The resistor in conventional CTLE is replaced with switched resistors and the tail current sources are replaced with clocked current sources as shown in **fig.2.** When CLK is high, the DTLE acts as a peaking amplifier where clocked current sources and the loading resistors are ON, and when CLK is low, the clocked current sources are OFF and the loading resistors are high impedance and thus holding the output values for the ADC during this phase.

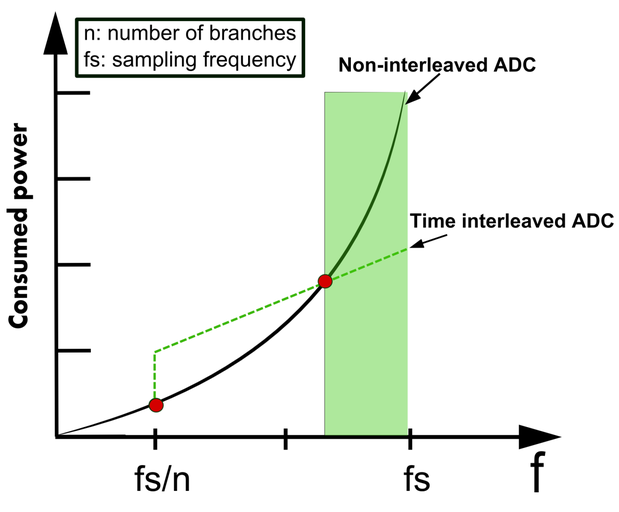


Fig. 1. Time-Interleaving Concept

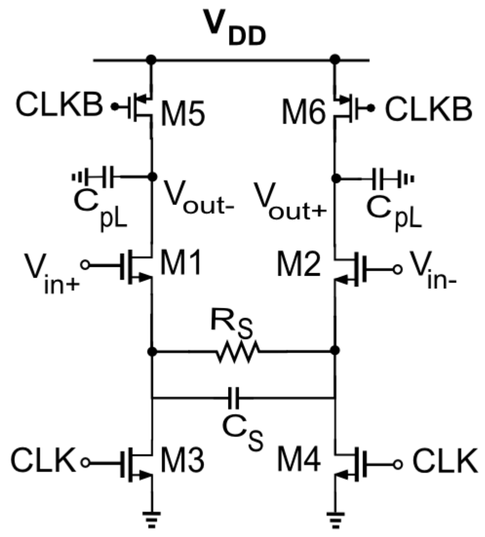


Fig. 2. DTLE Schematic

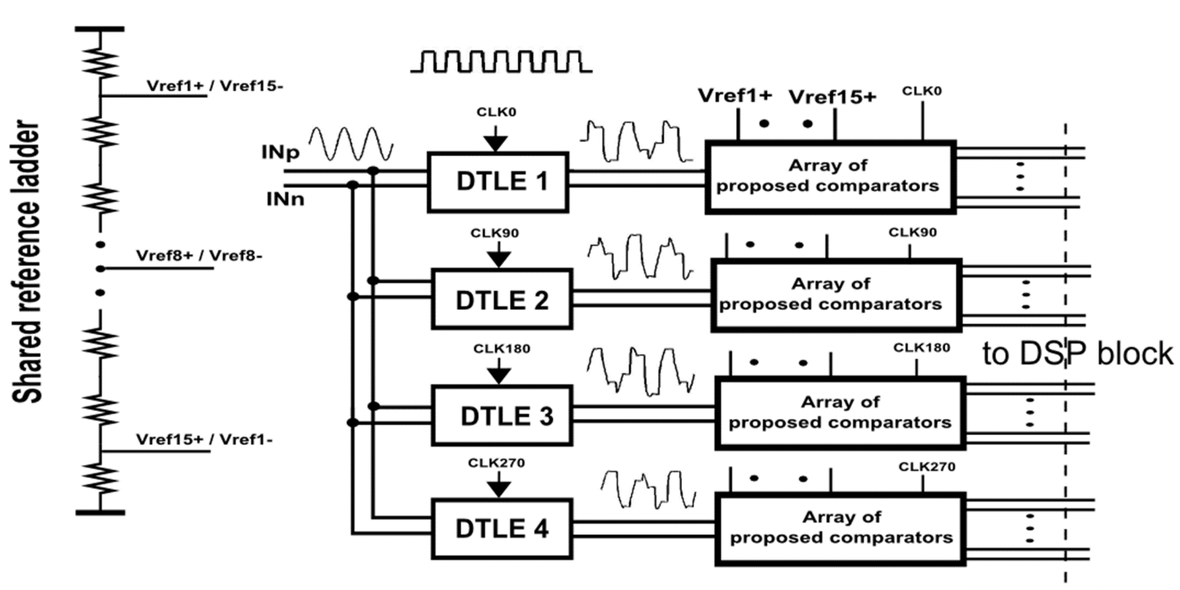


Fig. 3. Architecture of ADC-based Equalizer

ADC

4x interleaving ADC is used while all four channels share the reference ladder to reduce the total power consumption. Four 5 GHz clocks separated by 90 phase shifts are used with DTLEs at the input of the channels. The outputs are directly fed to the digital back-end of a serial-link receiver. ADC architecture is in **fig.3.** The proposed comparator consists of a dynamic charge-steering pre-amplifier with an embedded regenerative latch and its clocking scheme are shown in **fig. 4.** and **fig. 5**. respectively. comparator is shown in its all phases in **fig. 6.**

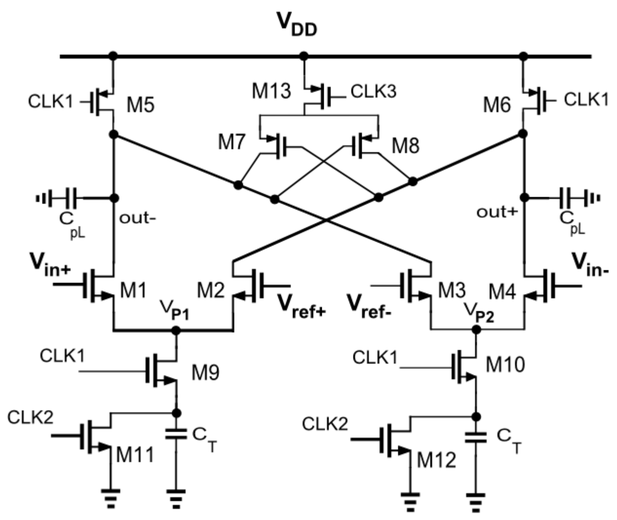


Fig.4. Proposed Comparator Circuit

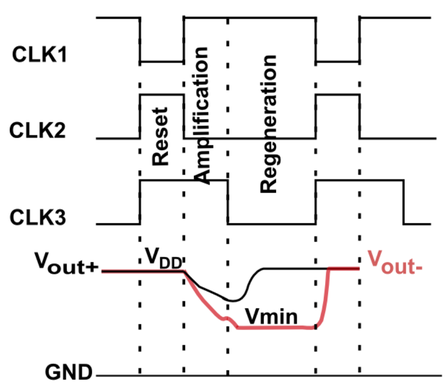


Fig.5. Clocking Scheme

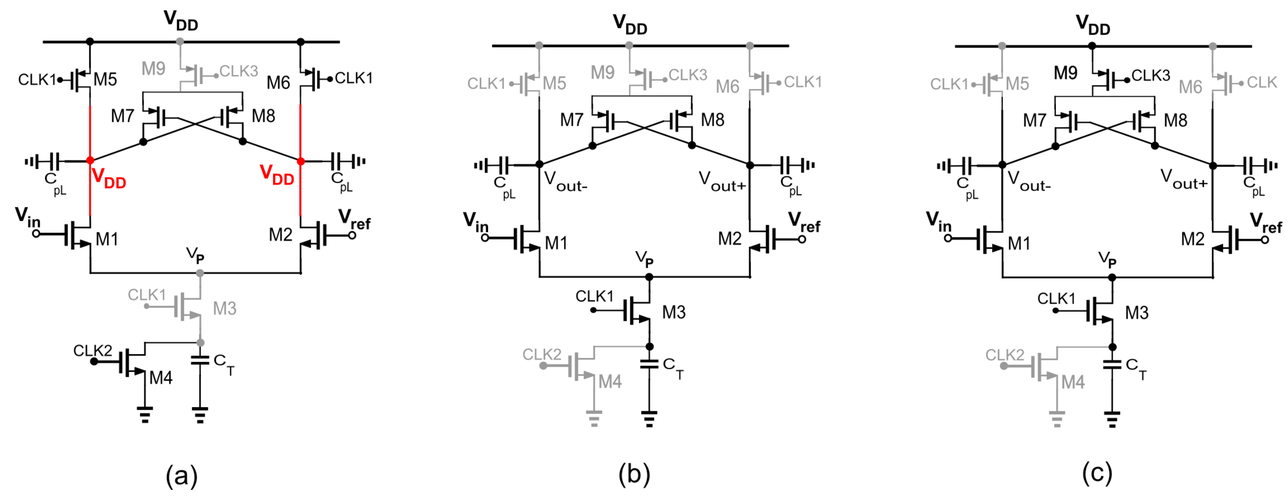
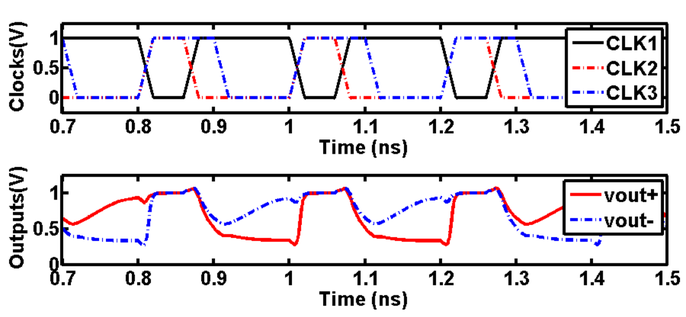
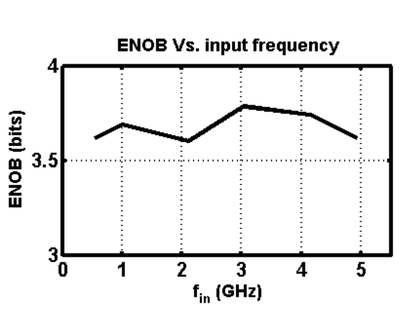


Fig.6. Different Phases for Proposed Comparator; (a) Reset Phase (b) Amplification Phase (c) Regeneration Phase



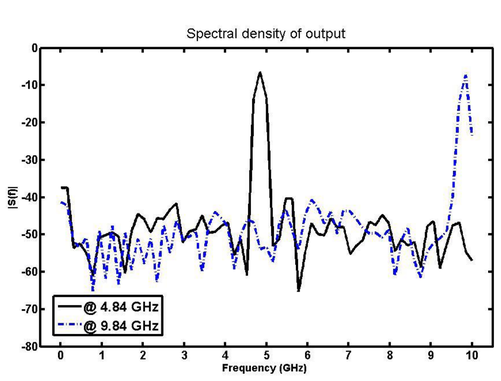


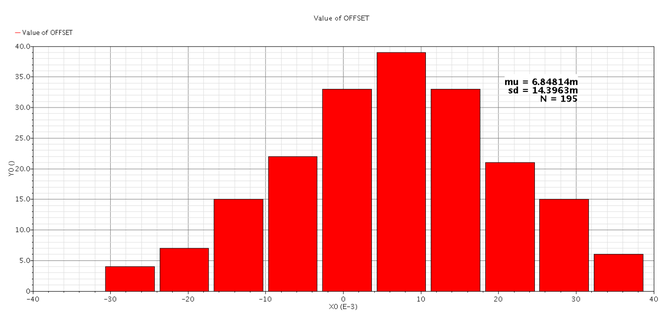
Simulation results

Simulation results are shown in fig. 7-9 and table 1, also Kick-back noise level is proved to be tiny because outputs of comparator core don't have rail to rail values, this allows us to increase the resistors value in the reference resistive ladder which results in lower power consumption in the ladder.

TABLE I. PERFORMANCE SUMMARY

Sampling frequency	20 GSPS
Input Range	600 mV_{diff}
SFDR	33.58 dB
SNDR	23.86 dB
ENOB (for 9.98GHz input frequency)	3.67 Bits
Power at Nyquist frequency	15.5 mW
FOMW*	60.8 fJ/conv-step





Conclusion

A 4-bit 20-GSps flash ADC is designed and simulated in TSMC 65-nm technology for ADC-based equalizer in serial links receiver. The power consumption is 16 mW. Four techniques are used to reduce the power consumption of the ADC-based equalizer; using the novel DTLE circuit, sharing the reference ladder between the four channels of ADC, using charge-steering concept for the comparator pre-amplification, and merging the regenerative latch inside the pre-amplifier while using charge redistribution in the regeneration phase without the need of a DC path to GND.

Acknowledgment

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