Mostafa A. Abouelkassem

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EDUCATION

The University of Southern California, Viterbi School of Engineering, Los Angeles, CA
Ph.D. Annenberg Fellow, Electrical Engineering, **GPA 4/4** Aug 2017 – Present
Coursework: Analog-Mixed Integrated Circuits (4/4), Quantum Mechanics (4/4),
Analog-Mixed Integrated Circuits 2 (4/4), Communications Integrated Circuits (4/4)
VLSI System Design (ongoing), Solid State Processing and Integrated Circuits Laboratory (ongoing)

Ain Shams University, Faculty of Engineering, Cairo, Egypt
M.Sc., Electrical Engineering, **GPA 3.5/4** Oct 2013 – May 2017
Coursework: Analog IC Design, Digital IC Design, RFIC Design, Power Management IC Design, and High-Speed Serial Links.
M.Sc. thesis: "A Low-power High-speed ADC-based Equalizer for Serial Links."

Alexandria University, Faculty of Engineering, Alexandria, Egypt
B.Sc., Electrical Engineering, Electronics Major, 93.44% equivalent to **GPA 3.96/4** Sept 2008 – July 2013
Distinction with degree of honor (5 years distinction), ranked **1st** over a 335-student class.

WORK EXPERIENCE

The University of Southern California, Viterbi School of Engineering, Los Angeles, CA
Graduate Research Assistant Aug 2017 – Present
- Working on low-power IC design.
- Taped-Out Ultra-Low-Power 8-Bit SAR ADC Sept. 2018

Skyworks Inc., Newbury Park, CA
Analog-Mixed IC Design Engineer Intern June 2018 – Aug 2018
- Worked in Advanced Mobile Solutions Division.
- Worked on PA Digital Controller and Bias Circuits.

Silicon Vision (Si-Vi), Synopsys Inc., Cairo, Egypt
Analog-Mixed IC Design Engineer Dec 2015 – July 2017
- Designed discrete-time and continuous-time comparators, and up-down counter.
- Worked on Analog verification of IO pads, loop-filter, VCO, feedback divider and calibration divider.

Integrated Circuits Lab (ICL), Ain Shams University, Cairo, Egypt
Research Assistant Sept 2013 – Nov 2015
- Worked on a low-power high-speed serial link ADC-based receiver.
- Responsible for the design of an ultra-low-power ADC and a front end CTLE equalizer.

Alexandria University, Faculty of Engineering, Alexandria, Egypt
Teaching Assistant Sept 2013 – July 2017
- Taught full lectures and labs in Circuits Analysis, Logic-Design, Electronics I and II,
Analog IC Design, Solid-State Physics, Solid-State Devices, 8086/8088 Microprocessor basics I and II.

CONSULTIX Systems, Cairo, Egypt
RF Board Level Design Engineer Intern Jan 2014 – Feb 2014
- Worked on Rectenna RF-DC Conversion and gained experience in ADS software.

Si-Ware Systems (SWS), Cairo, Egypt
Application Engineer Intern, ASIC solutions division Aug 2012 – Sept 2012
- Worked on testing SWS chips and gained experience in LabVIEW software.

CURRICULUM PROJECTS

Major Design Projects:
"An 8-bit Ultra-Low-Power SAR ADC for Bio-signals Applications" Oct 2017 – Present
- Ongoing project

"A 75-dB 100-MHz Signal-Bandwidth Continuous Time Delta-Sigma ADC" March 2018 – April 2018
- Built system-level simulations using both Verilog-A and Matlab for CIFF and CIFB architectures.
- Built 1.5bit Quantizer and 1.5bit Feedback DAC.

"A Low-Power 12-Gbps Multi-Standard SERDES Transceiver" (Funded by ITIDA) Sept 2013 – Nov 2015

- Designed an ultra-low-power ADC and a Discrete-Time Linear Equalizer (DTLE).
- Modeled a Digital DFE and an adaptive CTLE
- Finished post-layout simulations for 20-Gbps 15.5-mW ADC in UMC65 and built the chip I/O Pad ring.

"High-Speed Serial Link Transceiver for 10Gbase-KR Standard Using a 65-nm CMOS Process" Sept 2012 – June 2013

- Modeled a time-interleaved Flash ADC using Matlab Simulink
- Designed a 4-bit 10GS/s time-interleaved Flash ADC, Thermometer to binary digital encoder, and 1:16 Demultiplexer.
- Designed the digital RX system level.

Mini Design Projects:

"512-Bit SRAM Architecture Design" *Sept 2018*

- Build 4 banks of SRAM, Row Decoder, Column Decoder, Sense Amplifier
- All schematics to Layout, PEX and post-layout simulations

"A Differential 3.5-GHz Voltage Controlled Oscillator" Through April 2018

- Designed an LC-tank based Oscillator with 20% tuning range.
- Used digital bits and a varactor to tune the oscillation frequency.

"A Differential Switched-Capacitor Residue Amplifier for 12-bit 100 MS/s ADC" Through April 2018

- Analyze the different non-idealities in the SC amplifier and their effects.

"Zero/Low IF Wireless Receiver Frontend: LNA + Harmonic-Reject Quadrature Mixer" Through March 2018

- Designed an HRM using multi-phases clock.
- Achieved HR3 of 40.5dB, HR5 of 54.3dB and power of 9mA for the LNA and the Mixer.

"12-bit 200-MS/s 5-GHz Bandwidth Track and Hold Circuit" Through March 2018

- Built a driver for the sampling circuit
- Used a bootstrapped switch to get low distortion as possible
- Achieved $0.9Vpp$ input, SNDR of $75dB$ and SFDR of $95.2dB$

"An Inductor-less Wideband Low Noise Amplifier" Through Feb 2018

- Designed a Gm-boosted LNA using feedforward cancellation technique.
- Designed for low-gain and high-gain operation.

"A Rail-to-Rail Input / Output Current-Recycling Folded Cascode OTA in 45nm Process" Through Nov 2017

- Designed a two-stage OTA with a rail-to-rail input and output.
- Used miller and feedforward compensation.
- Achieved gain of $50dB$, GBW of $1.4GHz$, 60.2^o $P.M.$, $ICMR = 0.1 - 0.9V$ while consuming $6mW$

"A Design of eDRAM System Architecture" April 2015 – June 2015

- Designed 4T and 3T1D eDRAM cells, Sense Amplifier, Column Tree Decoder, and NOR Row Decoder.
- Used Fin-FET Verilog-A model from EECS Berkeley open library.

"A Design of Full 6-Gbps SERDES Link: Channel-Characterization, TX and RX" Dec 2014 – Jan 2015

- Designed CTLE, VGA, Sampler and SR Latch.

"A Design of SC Buck DC-DC Step-Down Converter" July 2014 – Aug 2014

- Designed Multi-ratio ($1, 3/4, 2/3, 4/5$) adaptive SC DC-DC converter to down convert 2.5V nominal line to 1.8V
- 38mV output ripples for 200mV input ripples, 30mΩ ESR and accuracy of 20mV

"A Design of Wideband Low-Noise Amplifier (LNA)" April 2014 – May 2014

- Designed a highly linear LNA with 18.25dB gain, 1dB NF, 2.2dBm IIP3.
- The total power consumption is 4.3mA. The LNA is operating from 200MHz to 2.45GHz

"Designing a Spiral, Coplanar and Microstrip Inductors Using Sonnet" April 2014 – May 2014

- Designed different types of integrated inductors with different quality factors.
- Gained experience in Sonnet software.

"A Model of a Simple System Level for Bluetooth System Using Simulink" Feb 2014 – March 2014

- Modeled a simple and abstractive Bluetooth system using ADC and Phase domain ADC.

"Design and Characterization of a CMOS 8-bit Microprocessor Data Path" Mar 2013 – June 2013

- Designed the behavioral model of an 8-bit microprocessor using Verilog.
- Designed the barrel shifter, latches and flip-flops & their layout using L-Edit.

"System Level Design of a Pipeline ADC" Sept 2012

- Modeled a 1.5bit M-DAC based Pipeline ADC using Matlab Simulink.
- Investigated building open-loop and closed-loop amplifier in each pipeline sub-stage.

"Behavioral Modeling for Serial Data Receiver Using VHDL" April 2011 – May 2011

- Designed a behavioral serial data RX that receives data chunks of 10 bits from a serial data bus. RX was modeled Using Xilinix, Modelsim and written in VHDL.

TECHNICAL SKILLS

- **Simulation Tools:** Cadence Virtuoso, MATLAB and Simulink, ADS, Synopsys analog flow, Sonnet, LabVIEW, Xilinx ISE, Quartus, Modelsim, PCB skills, Multisim, and Mentor Graphics (ELDO)
- **Layout:** Calibre (DRC, LVS, PEX), and L-Edit
- **Programming:** Verilog-AMS, VHDL, Shell Scripting, python, SKILL, C, and Assembly (for x86 series and MCS-51 family)
- **Lab instruments**: LPFKS62, Network Analyzer, NI-DAQ, Temperature Chamber, Oscilloscope, Multimeter, logic analyzer, and Function generator
- **Editing:** LATEX, Inkscape, and MS-Visio

- Underlined terms refer to a beginner-level experience

PUBLICATIONS

- **M. M. Ayesh**, S. Ibrahim and M. M. Aboudina, "*Design and Analysis of an Ultra-Low-Power Charge-Steering Based StrongARM Comparator*," ICM, 2016.
- **M. M. Ayesh**, "*A Low-power High-speed Charge-steering ADC-based Equalizer for Serial Links*," ICECS, M.Sc/Ph.D. Forum, December 2015.
- **M. M. Ayesh**, S. Ibrahim and M. M. Aboudina, "*15.5-mW 20-GSps 4-Bit Charge-Steering Flash ADC*," MWSCAS, pp.33-36, August 2015.

AWARDS

- Recipient of the **Annenberg Fellowship**, USC Viterbi School of Engineering (2017)
- Recipient of a full scholarship throughout M.Sc. studies. (2013-2016)
- Third place in M.Sc. Forum of the 2015 IEEE International Conference on Electronics, Circuits, and Systems for: "A Low-Power High-Speed Charge-Steering ADC-Based Equalizer for Serial Links".
- Recipient of Alexandria University annual academic **distinction award**. (2009-2013)

TECHNICAL SERVICES

- Reviewed papers for the IEEE International Symposium on Circuits and Systems (ISCAS) 2017, MWSCAS 2017, and Springer-Ain Shams Journal.
- Reviewed projects for IEEE Egypt section in 2015 EED (Egyptian Engineering Day).

EXTRACURRICULAR ACTIVITIES

VLSI-Egypt – Alexandria Section NGO, Alexandria, Egypt. Nov 2013 – Dec 2016
Founder and Chairman

EgyptScholars – Alexandria Student Branch NGO, Alexandria, Egypt Sept 2013 – Mar 2015
Founder and Chairman

IEEE – Alexandria Student Branch – SSCS, Alexandria, Egypt Sept 2013 – Mar 2015
Instructor for Basic Electronics & Analog Design courses

EWEB NGO, Alexandria, Egypt Sept 2013 – Dec 2014
Instructor for Basic Electronics & Analog Design courses